REMARKS

Examiner Arora is thanked for the thorough examination and search of the subject patent application.

Claims 1, 4, 7, 9-23, 25-27, 29-31, 40, 45, 48-51 and 76-79, 81-83, 88-107 are pending; Claims 1, 4, 7, 9-23, 25-27, 29-31, 40, 48-51 and 76-79, 81-83 and 89 have been currently amended; Claims 4, 29 and 30 have been withdrawn and currently amended; Claims 2, 3, 5, 6, 8, 24, 28, 32-39, 41-44, 46, 47, 52-75, 80, and 84-87 have been canceled; Claims 90-107 have been newly added. It is believed that no new matter is added.

The specification has been amended to correct a typing error of a reference number.

Response to Claim Rejections under 35 U.S.C. 112

Reconsiderations of Claims 1, 9, 15, 40, 76 and 83 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention are requested based on the following remarks.

Typically, a transistor, such as MOS device, comprises a first portion, such as ion diffusion layer, in a semiconductor substrate and a second portion, such as gate oxide, on or over the semiconductor substrate. It is believed that the description that "a transistor is in and over a semiconductor substrate" is adequate.

Withdrawal of Claim Rejection under 35 U.S.C 112 is respectfully requested.

Response to Claim Rejections under 35 U.S.C. 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 1, 4, 7 and 91-97

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As currently amended, independent Claim 1 is recited below:

1. An integrated circuit chip comprising:
a semiconductor substrate;
a transistor in and over said semiconductor substrate;
multiple metal and dielectric layers over said semiconductor substrate;
a passivation layer over said multiple metal and dielectric layers;
a power metal structure over said passivation layer, wherein said power metal structure comprises a copper layer;

a ground metal structure over said passivation layer, wherein said ground metal structure comprises a copper layer;

a capacitor over said passivation layer;

a first solder connection connecting said capacitor to said power metal structure; and

a second solder connection connecting said capacitor to said ground metal structure.

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Reconsiderations of Claims 1, 2 and 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US6,303,423) and of Claims 3, 5, 6 and 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Nakanishi et al. (US6,921,980) are requested based on the following remarks.

Applicants respectfully assert that the integrated circuit chip claimed in Claim 1 patentably distinguishes over the citation by Lin (US6,303,423).

Lin teaches "Semiconductor devices that have been provided in the surface of substrate 10 can, via the conductive interconnects contained in opening 22/36/38, be further connected to surrounding components and circuitry". ~ *See col. 8, lines 13-19* ~ However, Lin fails to teach the surrounding components and circuitry may comprise a capacitor connected to a power metal structure and a ground metal structure through two solder connections, respectively, as claimed in Claim 1.

The Examiner considers that "The embodiment of Figure 10 of Lin utilizes a substrate similar to that of Figure 1, wherein the electronic component (54) over said semiconductor substrate (10) may be a capacitor (Col. 14, lines 22-23), and the connections (52) of the capacitor are solder connections (Col. 14, lines 16-21)", "It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the embodiment of Figure 1 of Lin so that the electronic component is a capacitor and that the connections to the power bus and ground bus is by solder connections", "The ordinary artisan would be motivated to modify Lin at least for the purpose of reducing parasitics in the circuit component (col. 7, lines 19-24) while using an attachment material like solder which provides good adhesion at a process temperature compatible with a wide variety of circuit component manufacturing processes". *~ See lines 7-18, on page 4, in the last Office Action mailed May 4, 2007 ~*

Applicants respectfully traverse the Examiner's opinion because it is believed to be unobvious to one of ordinary skill in the art at the time the invention was made to modify the embodiment of Figure 1 of Lin so that the surrounding components and circuitry may comprise a capacitor connected to a power metal structure and a ground metal structure through two solder connections, respectively. Even though the embodiments in Figs. 1 and 10 could be combined, those skilled in the art at the time the invention was made could come up with a capacitor that can be mounted over a semiconductor substrate, but have no idea what kind of contact points may be connected to a capacitor through solder connections because Lin fails to teach a capacitor over a semiconductor substrate may be

connected to a power metal structure and a ground metal structure through two solder connections, respectively, as claimed in Claim 1.

Withdrawal of the Claim Rejection under 35 U.S.C. 103(a) to Claim 1 is respectfully requested.

Applicants respectfully submit independent Claim 1 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 4, 7 and 91-97 patentably define over the prior art as well.

Response to Claims 9-14 and 98-100

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As currently amended, independent Claim 9 is recited below:

9. An integrated circuit chip comprising:
a semiconductor substrate;
a transistor in and over said semiconductor substrate;
multiple metal and dielectric layers over said semiconductor substrate;
a passivation layer over said multiple metal and dielectric layers, a first opening in said passivation layer exposing a first contact pad of said multiple metal and dielectric layers, wherein said passivation layer comprises nitride;
a second contact pad connected to said first contact pad through said first opening, wherein the position of said second contact pad from a top perspective view is different from that of said first contact pad, wherein said second contact pad comprises a gold layer;
a capacitor over said passivation layer; and
a solder connection connecting said capacitor to said second contact pad.

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Reconsiderations of Claims 9, 13 and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US6,303,423) and of Claims 10-12 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Nakanishi et al. (US6,921,980) are requested based on the following remarks.

Applicants respectfully assert that the integrated circuit chip claimed in Claim 9 patentably distinguishes over the citation by Lin (US6,303,423).

Lin teaches "Semiconductor devices that have been provided in the surface of substrate 10 can, via the conductive interconnects contained in opening 22/36/38, be further connected to surrounding components and circuitry". ~ *See col. 8, lines 13-19* ~ However, Lin fails to teach the surrounding components and circuitry may comprise a capacitor connected to a second contact pad connected to a first contact pad exposed by an opening in a passivation layer, wherein the position of the second contact pad from a top perspective view is different from that of the first contact pad, as claimed in Claim 9.

The Examiner considers that "The embodiment of Figure 10 of Lin utilizes a substrate similar to that of Figure 1, wherein the electronic component (54) over said semiconductor substrate (10) may be a capacitor (Col. 14, lines 22-23)", "It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the embodiment of Figure 1 of Lin so that the electronic component is a capacitor",

"The ordinary artisan would be motivated to modify Lin at least for the purpose of reducing parasitics in the circuit component (col. 7, lines 19-24)". ~ *See lines 4-10, on page 6, in the last Office Action mailed May 4, 2007* ~

Applicants respectfully traverse the Examiner's opinion because it is believed to be unobvious to one of ordinary skill in the art at the time the invention was made to modify the embodiment of Figure 1 of Lin so that the surrounding components and circuitry may comprise a capacitor connected to a second contact pad connected to a first contact pad exposed by an opening in a passivation layer, wherein the position of the second contact pad from a top perspective view is different from that of the first contact pad. Lin fails to teach where is the exact position of a second contact pad 26 or 28, in Fig. 1, to be connected to a surrounding component, but only teach a second contact pad 50, in Fig. 10, to be connected to a capacitor 54 is over a first contact pad 16 exposed by an opening in a passivation layer 18. Even though the embodiments in Figs. 1 and 10 could be combined, those skilled in the art at the time the invention was made could come up with a capacitor that can be mounted over a second contact pad over a first contact pad exposed by an opening in a passivation layer, but have no idea that the position of the second contact pad from a top perspective view is different from that of the first contact pad, as claimed in Claim 9.

Withdrawal of the Claim Rejection under 35 U.S.C. 103(a) to Claim 9 is respectfully requested.

Applicants respectfully submit independent Claim 9 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 10-14 and 98-100 patentably define over the prior art as well.

Response to Claims 15-23, 25-27, 29-31 and 101-104

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As currently amended, independent Claim 15 is recited below:

15. An integrated circuit chip comprising:
a semiconductor substrate;
a transistor in and over said semiconductor substrate;
multiple metal and dielectric layers over said semiconductor substrate;
a passivation layer over said multiple metal and dielectric layers;
a first metal pad over said semiconductor substrate;
a second metal pad having a portion over said passivation layer, wherein said second metal pad is used to be wirebonded thereto;
a capacitor over said passivation layer; and
a solder connection connecting said capacitor to said first metal pad.

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Reconsiderations of Claims 15, 17-19, 21, 22, 24-25, 27 and 31 rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi et al. (US6,921,980) in view of Lin (US6,303,423), of Claims 16, 20 and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi et al. in view of Lin and further in view of Murdeshwar, of Claim 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi et al. in view of Lin and further in view of Greer (US6,451,681), and of Claim 28 rejected under 35

U.S.C. 103(a) as being unpatentable over Nakanishi et al. in view of Lin and further in view of Thomas et al. (US5,346,858) are requested based on the following remarks.

Applicants respectfully assert that the integrated circuit chip claimed in Claim 15 patentably distinguishes over the citations by Nakanishi et al. (US6,932,980) in view of Lin (US6,303,423).

Nakanishi et al. teach a component connection terminal 7 made of solder connects a discrete electronic component 8 to a pad of a semiconductor chip 2. ~ *See Fig. 2E; col. 3, lines 58-64; col. 4, lines 5 and 6* ~ However, Nakanishi et al. fail to teach that the discrete electronic component 8 may be a capacitor.

Nakanishi et al. fail to teach, hint or suggest the subject matter that a solder connection connects a capacitor to a pad over a semiconductor substrate, as claimed in Claim 15.

The Examiner considers that "Lin (refer to Figure 10) teaches a circuit component comprising a semiconductor substrate with an electronic component over said semiconductor substrate, wherein the electronic component (54) may be a capacitor (Col. 14, lines 22-23)", "It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakanishi so that the electronic component is a

capacitor", and "The ordinary artisan would be motivated to modify Nakanishi for at least the purpose of reducing parasitics in the circuit component (Col. 7, lines 19-24)".

Applicants respectfully traverse the Examiner's opinion because it is believed to be unobvious to one of ordinary skill in the art at the time the invention was made to modify the Nakanishi et al's device so that the discrete electronic component is a capacitor. Lin teaches a capacitor 54 may be connected to a pad 16 exposed by an opening in a passivation layer 18, but fails to teach the capacitor 54 over a semiconductor chip can be connected to an external circuit. Therefore, based on Lin's teaching, those skilled in the art would not come up with a capacitor that can be connected to an external circuit. It is believed that the capacitor 54 in Lin's device is not analogous to the discrete electronic component 8 in Nakanishi et al's device connected to an external circuit.

Withdrawal of the Claim Rejection under 35 U.S.C. 103(a) to Claim 15 is respectfully requested.

Applicants respectfully submit independent Claim 15 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 16-23, 25-27, 29-31 and 101-104 patentably define over the prior art as well.

Response to Claims 40, 45, 48-51 and 105

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As currently amended, independent Claim 40 is recited below:

40. A method of fabricating an integrated circuit chip, comprising:
providing a semiconductor substrate, a transistor in and over said semiconductor substrate, multiple metal and dielectric layers over said semiconductor substrate, and a passivation layer over said multiple metal and dielectric layers, an opening in said passivation layer exposing a first contact pad of said multiple metal and dielectric layers, wherein said passivation layer comprises silicon nitride;
forming a second contact pad over said passivation layer, wherein said second contact pad is connected to said first contact pad through said opening, and the position of said second contact pad from a top view is different from that of said first contact pad, wherein said forming said second contact pad comprises an electroplating process; and
mounting a capacitor over said passivation layer, wherein an electrode of said capacitor is directly over and connected to said second contact pad.

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Reconsiderations of Claims 40-45, 49 and 50 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US6,303,423), of Claim 48 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Nakanishi et al. (US6,921,980), of Claim 47 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Greer (US6,451,681) and of Claim 51 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Jiang et al. (US2003/0119299) are requested based on the following remarks.

Applicants respectfully assert that the method claimed in Claim 40 patentably distinguishes over the citation by Lin (US6,303,423).

Lin teaches "Semiconductor devices that have been provided in the surface of substrate 10 can, via the conductive interconnects contained in opening 22/36/38, be further connected to surrounding components and circuitry". ~ *See col. 8, lines 13-19* ~ However, Lin fails to teach the surrounding components and circuitry may comprise a capacitor mounted to a second contact pad connected to a first contact pad exposed by an opening in a passivation layer, wherein the position of the second contact pad from a top perspective view is different from that of the first contact pad, as claimed in Claim 40.

The Examiner considers that "The embodiment of Figure 10 of Lin utilizes a substrate similar to that of Figure 1, wherein the electronic component (54) over said semiconductor substrate (10) may be a capacitor (Col. 14, lines 22-23)", "It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the embodiment of Figure 1 of Lin so that the electronic component is a capacitor", "The ordinary artisan would be motivated to modify Lin at least for the purpose of reducing parasitics in the circuit component (col. 7, lines 19-24)". ~ *See line 19 of page 7 through line 5 of page 8, in the last Office Action mailed May 4, 2007* ~

Applicants respectfully traverse the Examiner's opinion because it is believed to be unobvious to one of ordinary skill in the art at the time the invention was made to modify the embodiment of Figure 1 of Lin so that the surrounding components and circuitry may comprise a capacitor mounted to a second contact pad connected to a first contact pad exposed by an opening in a passivation layer, wherein the position of the second contact pad from a top perspective view is different from that of the first contact pad. Lin fails to

teach where is the exact position of a second contact pad 26 or 28, in Fig. 1, to be connected to a surrounding component, but only teach a second contact pad 50, in Fig. 10, to be connected to a capacitor 54 is over a first contact pad 16 exposed by an opening in a passivation layer 18. Even though the embodiments in Figs. 1 and 10 could be combined, those skilled in the art at the time the invention was made could come up with a capacitor that can be mounted over a second contact pad over a first contact pad exposed by an opening in a passivation layer, but have no idea that the position of the second contact pad from a top perspective view is different from that of the first contact pad, as claimed in Claim 40.

Withdrawal of the Claim Rejection under 35 U.S.C. 103(a) to Claim 40 is respectfully requested.

Applicants respectfully submit independent Claim 40 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 45, 48-51 and 105 patentably define over the prior art as well.

Response to Claims 76-79, 81, 82, 106 and 107

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As currently amended, independent Claim 76 is recited below:

76. A method of fabricating an integrated circuit chip comprising:
providing a semiconductor substrate, a transistor in and over said semiconductor substrate, multiple metal and dielectric layers over said semiconductor substrate, a passivation layer over said multiple metal and dielectric layers, a first contact pad over said semiconductor substrate, and a second contact pad having a portion over said passivation layer, wherein said second contact pad is used to be wirebonded thereto; and
mounting a capacitor over said passivation layer, wherein an electrode of said capacitor is directly over and connected to said first contact pad.
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Reconsiderations of Claims 76-82 rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi et al. (US6,921,980) in view of Lin (US6,303,423) are requested based on the following remarks.

Applicants respectfully assert that the method claimed in Claim 76 patentably distinguishes over the citations by Nakanishi et al. (US6,932,980) in view of Lin (US6,303,423).

Nakanishi et al. teach a discrete electronic component 8 mounted to a pad of a semiconductor chip 2. ~ *See Fig. 2E; col. 3, lines 58-64; col. 4, lines 5 and 6* ~ However, Nakanishi et al. fail to teach that the discrete electronic component 8 may be a capacitor.

Nakanishi et al. fail to teach, hint or suggest the subject matter that a solder connection connects a capacitor to a pad over a semiconductor substrate, as claimed in Claim 15.

The Examiner considers that "Lin (refer to Figure 10) teaches a circuit component comprising a substrate with an electronic component over said semiconductor substrate, wherein the electronic component (54) may be a capacitor (Col. 14, lines 22-23)", "It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nakanishi so that the electronic component is a capacitor", and "The ordinary artisan would be motivated to modify Nakanishi for at least the purpose of reducing parasitics in the circuit component (Col. 7, lines 19-24)".

Applicants respectfully traverse the Examiner's opinion because it is believed to be unobvious to one of ordinary skill in the art at the time the invention was made to modify the Nakanishi et al's device so that the discrete electronic component is a capacitor. Lin teaches a capacitor 54 may be mounted to a pad 16 exposed by an opening in a passivation layer 18, but fails to teach the capacitor 54 over a semiconductor chip can be connected to an external circuit. Therefore, based on Lin's teaching, those skilled in the art would not come up with a capacitor that can be connected to an external circuit. It is believed that the capacitor 54 in Lin's device is not analogous to the discrete electronic component 8 in Nakanishi et al's device connected to an external circuit.

Withdrawal of the Claim Rejection under 35 U.S.C. 103(a) to Claim 76 is respectfully requested.

Applicants respectfully submit independent Claim 76 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 77-79, 81, 82, 106 and 107 patentably define over the prior art as well.

Response to Claims 83 and 88-90

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As currently amended, independent Claim 83 is recited below:

83. A method of fabricating an integrated circuit chip comprising:
providing a semiconductor substrate, a transistor in and over said semiconductor substrate, multiple metal and dielectric layers over said semiconductor substrate, and a passivation layer over said multiple metal and dielectric layers;
forming power and ground metal structures over said passivation layer, wherein said forming said power and ground metal structures comprises depositing a copper layer; and
mounting a capacitor over said passivation layer, wherein said mounting said capacitor comprises a printing process, and wherein said capacitor comprises a first electrode connected to said power metal structure, and a second electrode connected to said ground metal structure.

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Reconsiderations of Claims 83-87 and 89 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US6,303,423) and of Claim 88 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Nakanishi et al. (US6,921,980) are requested based on the following remarks.

Applicants respectfully assert that the method claimed in Claim 83 patentably distinguishes over the citation by Lin (US6,303,423).

Lin teaches "Semiconductor devices that have been provided in the surface of substrate 10 can, via the conductive interconnects contained in opening 22/36/38, be further connected to surrounding components and circuitry". ~ *See col. 8, lines 13-19* ~ However, Lin fails to teach the surrounding components and circuitry may comprise a capacitor mounted to power and ground metal structures, as claimed in Claim 83.

The Examiner considers that "The embodiment of Figure 10 of Lin utilizes a semiconductor substrate similar to that of Figure 1, wherein the electronic component (54) over said semiconductor substrate (10) may be a capacitor (Col. 14, lines 22-23)", "It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the embodiment of Figure 1 of Lin so that the electronic component is a capacitor", "The ordinary artisan would be motivated to modify Lin at least for the purpose of reducing parasitics in the circuit component (Col. 7, lines 19-24)". ~ *See lines 12-18, on page 11, in the last Office Action mailed May 4, 2007* ~

Applicants respectfully traverse the Examiner's opinion because it is believed to be unobvious to one of ordinary skill in the art at the time the invention was made to modify the embodiment of Figure 1 of Lin so that the surrounding components and circuitry may comprise a capacitor mounted to power and ground metal structures. Even though the

embodiments in Figs. 1 and 10 could be combined, those skilled in the art at the time the invention was made could come up with a capacitor that can be mounted over a semiconductor substrate, but have no idea what kind of contact points may be connected to a capacitor because Lin fails to teach a capacitor may be mounted to power and ground metal structures over a semiconductor substrate, as claimed in Claim 83.

Withdrawal of the Claim Rejection under 35 U.S.C. 103(a) to Claim 83 is respectfully requested.

Applicants respectfully submit independent Claim 83 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 88-90 patentably define over the prior art as well.

CONCLUSION

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should Examiner Arora not find that the Claims are now Allowable that he call the undersigned at 845 452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

Stephen B. Ackerman, Reg. No. 37,761